IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Baily, et al.	Docket No.:	ROC920030218US1
Serial No.:	10/616,683	Group Art Unit:	2112
Filed:	07/10/03	Examiner:	Stiglic, Ryan M.

For: COMPUTER APPARATUS AND METHOD FOR AUTONOMICALLY DETECTING SYSTEM CONFIGURATION AND MAINTAINING PERSISTENT I/O BUS NUMBERING

REPLY BRIEF

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Reply Brief is filed to address issues raised in the Examiner's Answer dated 6/7/06.

ARGUMENT

Issue 1: Whether claims 1-16 and 19-20 are unpatentable under 35 U.S.C. §103(a) over applicant's admitted prior art (AAPA) in view of Mizukami (US 2002/0120708A1).

The Examiner rejected the pending claims as being unpatentable over AAPA in view of Mizukami. Applicant traverses the Examiner's finding of obviousness of claims 1-16 and 19-20. The cited art individually or in combination does not teach or suggest the claimed invention herein.

Response to the Examiner's Answer

Applicants affirm the arguments made in the Appeal Brief filed on 04/10/2006, which is incorporated herein by reference. In the Examiner's answer, the Examiner makes the following characterization of the applicants admitted prior art (AAPA):

"Thus an inefficient failure recovery procedure (i.e. recovery from an upgrade) is evident and there exists a need for an efficient recovery procedure that provides Tower C with the ability to rollback to the configuration of Tower C prior to the failure event." (Last sentence of page 3 to page 4)

This statement by the Examiner is conclusory, and suffers from hindsight reconstruction. The AAPA does not suggest that the solution is to "roll back to the configuration of tower C." This conclusion is derived from Applicant's description of the invention, not the AAPA. The AAPA merely described the problem with assigning bus numbers in non-volatile memory when the system requires bus reconfiguration due to reconfiguration of the system arising from a hardware upgrade or hardware failure. In the prior art, bus numbering information was stored in local, non-volatile memory. When reconfiguration occurred, the previously used bus numbers would not be re-assigned. The solution to reconstruct the bus numbering of a tower is described in the Applicant's description of

the invention, not the AAPA. The above conclusory statement of the prior art is clearly tainted with hindsight from the applicant's disclosure and demonstrates how the Examiner has relied on hindsight reconstruction to build a case of obviousness. The above statement is used by the Examiner to make the jump between the AAPA and Mizukami, but since it is tainted with hindsight reconstruction, the conclusions drawn from this relationship are similarly tainted. The Examiner has failed to establish a prima facie case. Applicant hereby respectfully request the Examiner's final rejection of the pending claims under 35 U.S.C. §103(a) be reversed.

The Examiner further characterizes Mizukami at page 4, lines 11-13 of the Examiner's Answer as follows:

> Upon the loss of the configuration data of a node (e.g. a failure event) the data stored in the backup memory of an adjacent node is transferred to the failed node ([0023; 0083; 0085; 0095-0099]).

This statement shows the Examiner interprets Mizukami to teach the configuration data from the memory backup is "transferred" to the failed node. This makes sense in Mizukami and the type of failure that Mizukami overcomes. However, in the claimed invention, the bus numbering information is read to determine an appropriate bus number for a bus in the reconfigured enclosure (e.g. see claim 4). The data is not transferred to the failed node. In contrast, bus numbering information is used by the bus number manager to set up bus numbering. Further, the bus numbering that is re-configured is not in the "failed node" but in the replacement of the failed node. While this second difference is not in the claims explicitly, it is the nature of the invention and is significant with respect to the Examiner's broad interpretation of the similarities between the claimed invention and the prior art (AAPA and Mizukami). These differences between the prior art and the claimed invention are not properly addressed by the Examiner.

Further, the Examiner's answer continues to focus on the idea of failure event to broadly scope the AAPA and Mizukami to find obviousness. However, the claims

include a bus number manager that detects a change in configuration. The bus number manager then uses the stored bus numbering information to configure bus numbering while re-using the bus numbers. The Examiner has not shown how one of ordinary skill in the art would associate a change in configuration with a failure event in Mizukami. While a change in configuration may be the result of a failure, it is not a failure event that the bus number manager detects. In contrast, in Mizukami, the configuration data is restored to the failed node after a failure event. Mizukami in combination with the AAPA does not teach or suggest detecting a change in configuration to initiate access to the stored bus numbering information to reconfigure the system.

After making a broad interpretation of the claims and then associating them loosely with Mizukami, the Examiner has cobbled together an argument for obviousness. But these broad interpretations and associations leave several gaps that lack a motivation to combine the art in the specific manner as claimed, or the gaps are filled by hindsight reconstruction. The Examiner has failed to demonstrate how one of ordinary skill in the art would be motivated to make these vague associations and interpretations given the many differences between the claimed invention and the prior art. Recognizing that Mizukami is even related to the present invention requires hindsight. There is nothing in the AAPA or Mizukami to suggest that there is a benefit to combine the two in the manner of the present invention. Applicant respectfully requests the Examiner's final rejection of the pending claims under 35 U.S.C. §103(a) be reversed.

CONCLUSION

Claims 1-16 and 19-20 are addressed in this Appeal. For the numerous reasons articulated above, applicants maintain that the rejections of claims 1-16 and 19-20 under 35 U.S.C. § 103(a) are erroneous.

Applicants respectfully submit that this Reply Brief fully responds to, and successfully contravenes, every ground of rejection in the Examiner's Answer and respectfully requests that the final rejection be reversed and that all claims in the subject patent application be found allowable.

Respectfully submitted,

/bretjpetersen/
Bret J. Petersen
Reg. No. 37,417

MARTIN & ASSOCIATES, L.L.C.
P.O. Box 548
Carthage, MO 64836-0548
(417) 358-4700
Fax (417) 358-5757

CLAIMS APPENDIX

1. A first apparatus comprising:
a non-volatile memory that contains:
(A) bus numbering information for at least one bus located within the first apparatus; and
(B) bus numbering information for at least one bus located within a second apparatus coupled to the first apparatus.

2. The first apparatus of claim 1 wherein the bus numbering information comprises a beginning bus number and a number of buses.

3. The first apparatus of claim 1 wherein the non-volatile memory comprises at least one identifier for determining if contents of the non-volatile memory are valid.

4. A computer system comprising:

a first physical enclosure;

a second physical enclosure coupled to the first physical enclosure, the second physical enclosure including a non-volatile memory that contains bus numbering information for buses contained in the first and second physical enclosures; and

a bus number manager that detects a change in configuration of the computer system and that reads the bus numbering information from the non-volatile memory for the first and second physical enclosures to determine an appropriate bus number for at least one bus in the first and second physical enclosures.

5. The computer system of claim 4 wherein the bus numbering information comprises a beginning bus number and a number of buses.

6. The computer system of claim 4 wherein the non-volatile memory comprises at least one identifier that is read by the bus number manager to determine if contents of the non-volatile memory are valid.

7. A computer system comprising:

(1) a first physical enclosure comprising:

at least one processor;

a memory coupled to the at least one processor;

a non-volatile memory coupled to the at least one processor, the non-volatile memory including a bus number mask that indicates bus numbers in use in the computer system; and

a hub coupled to the at least one processor;

(2) a second physical enclosure comprising:

at least one bridge coupled to the hub in the first physical enclosure;

at least one numbered bus coupled to the at least one bridge;

a non-volatile memory that contains:

(A) bus numbering information for numbered buses in the second physical enclosure; and

(B) bus numbering information for numbered buses in a third physical enclosure;

(3) the third physical enclosure comprising:

at least one bridge coupled to the at least one bridge in the second physical enclosure;

at least one numbered bus coupled to the at least one bridge in the third physical enclosure;

a non-volatile memory that contains:

(A) bus numbering information for numbered buses in the third physical enclosure; and

(B) bus numbering information for numbered buses in the second physical enclosure;

(claim 7 continued)

(4) a bus number manager residing in the memory of the first physical enclosure and executed by the at least one processor in the first physical enclosure, the bus number manager detecting a change in configuration of the computer system and reading the bus numbering information from the non-volatile memory in the second and third physical enclosures to determine an appropriate bus number for at least one bus in the second and third physical enclosures.

8. The computer system of claim 7 wherein the bus numbering information comprises a beginning bus number and a number of buses.

9. A computer-implemented method for storing bus numbering information in a non-volatile memory, the method comprising the steps of:

assigning unique bus numbers to buses in a first physical enclosure;

assigning unique bus numbers to buses in a second physical enclosure; and

storing the bus numbers for the buses in the first and second physical enclosures in the non-volatile memory.

10. The method of claim 9 wherein the non-volatile memory resides in the first physical enclosure.

11. The method of claim 9 wherein the bus numbering information comprises a beginning bus number and a number of buses.

12. A computer-implemented method for numbering a plurality of buses in a computer system that includes a plurality of physical enclosures, the method comprising the steps of:

storing in a non-volatile memory bus numbering information for at least one bus in a first physical enclosure;

storing in the non-volatile memory bus numbering information for at least one bus in a second physical enclosure;

detecting a change in the computer system configuration; and

reading the bus numbering information from the non-volatile memory for the first and second physical enclosures to determine an appropriate bus number for at least one bus in the first and second physical enclosures.

13. The method of claim 12 wherein the bus numbering information comprises a beginning bus number and a number of buses.

14. A computer-implemented method for assigning and maintaining persistent numbers to a plurality of buses in a computer system that includes a plurality of physical enclosures, the method comprising the steps of:

assigning unique bus numbers to buses in a first physical enclosure;

assigning unique bus numbers to buses in a second physical enclosure coupled to the first physical enclosure;

storing bus numbering information corresponding to the bus numbers for the buses in the first and second physical enclosures in a first non-volatile memory in the first physical enclosure;

storing bus numbering information corresponding to the bus numbers for the buses in the first and second physical enclosures in a second non-volatile memory in the second physical enclosure;

detecting a change in the computer system configuration;

reading the bus numbering information from the first and second non-volatile memories to determine an appropriate bus number for the buses in the first physical enclosure; and

reading the bus numbering information from the first and second non-volatile memories to determine an appropriate bus number for the buses in the second physical enclosure.

15. The method of claim 14 wherein the bus numbering information comprises a beginning bus number and a number of buses.

16. A program product comprising:

a bus number manager that detects a change in configuration of a computer system that includes a plurality of physical enclosures, the bus number manager reading bus numbering information from a non-volatile memory in a first physical enclosure to determine an appropriate bus number for at least one bus in the first physical enclosure and at least one bus in a second physical enclosure; and

recordable signal bearing media bearing the bus number manager.

17. (Cancelled)

18. (Cancelled)

19. The program product of claim 16 wherein the bus numbering information comprises a beginning bus number and a number of buses.

20. The program product of claim 16 wherein the non-volatile memory comprises at least one identifier that is read by the bus number manager to determine if contents of the non-volatile memory are valid.

EVIDENCE APPENDIX

An Evidence Appendix is not required for this Reply Brief.

RELATED PROCEEDINGS APPENDIX

A Related Proceedings Appendix is not required for this Reply Brief.